Figure 1(a)

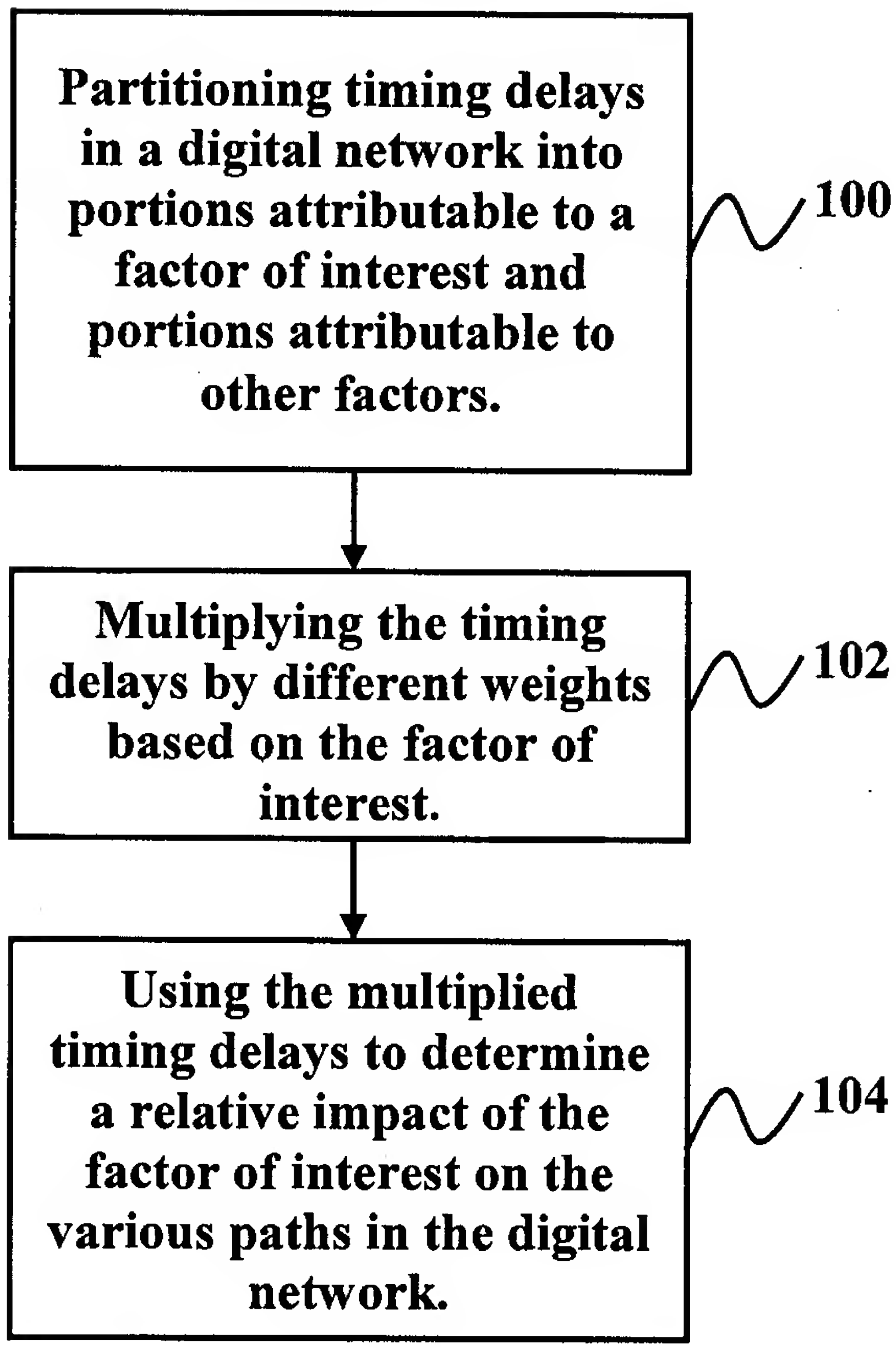


Figure 1(b)

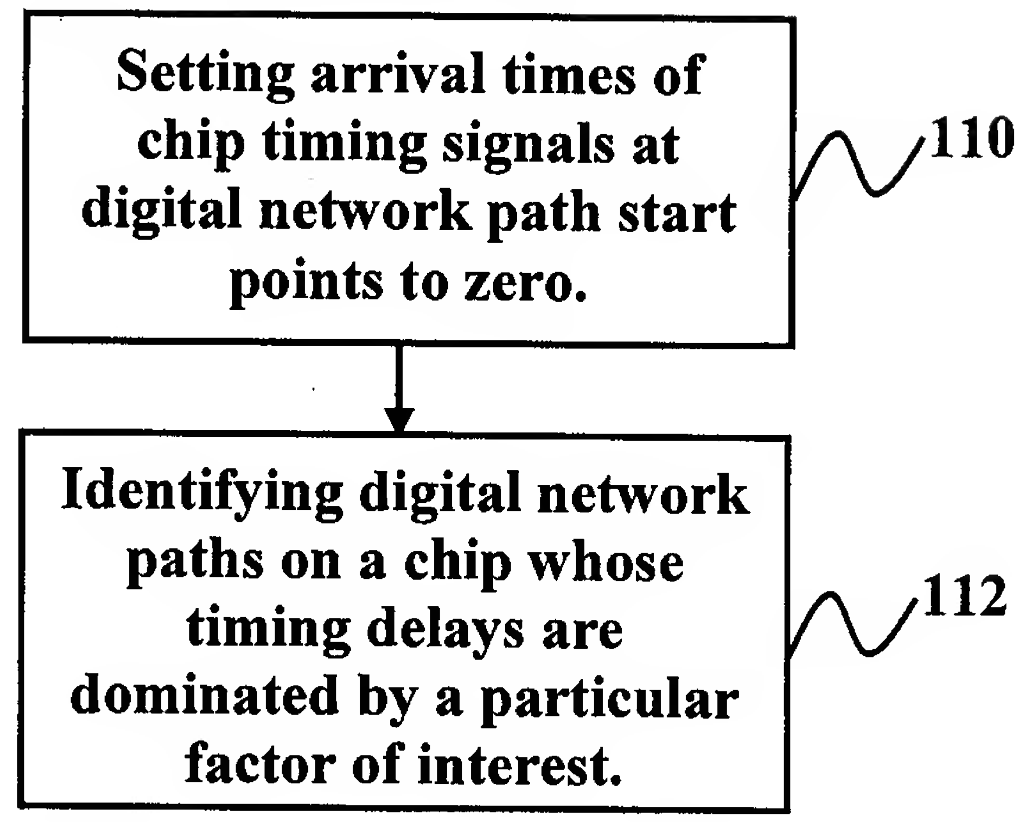


Figure 1(c)

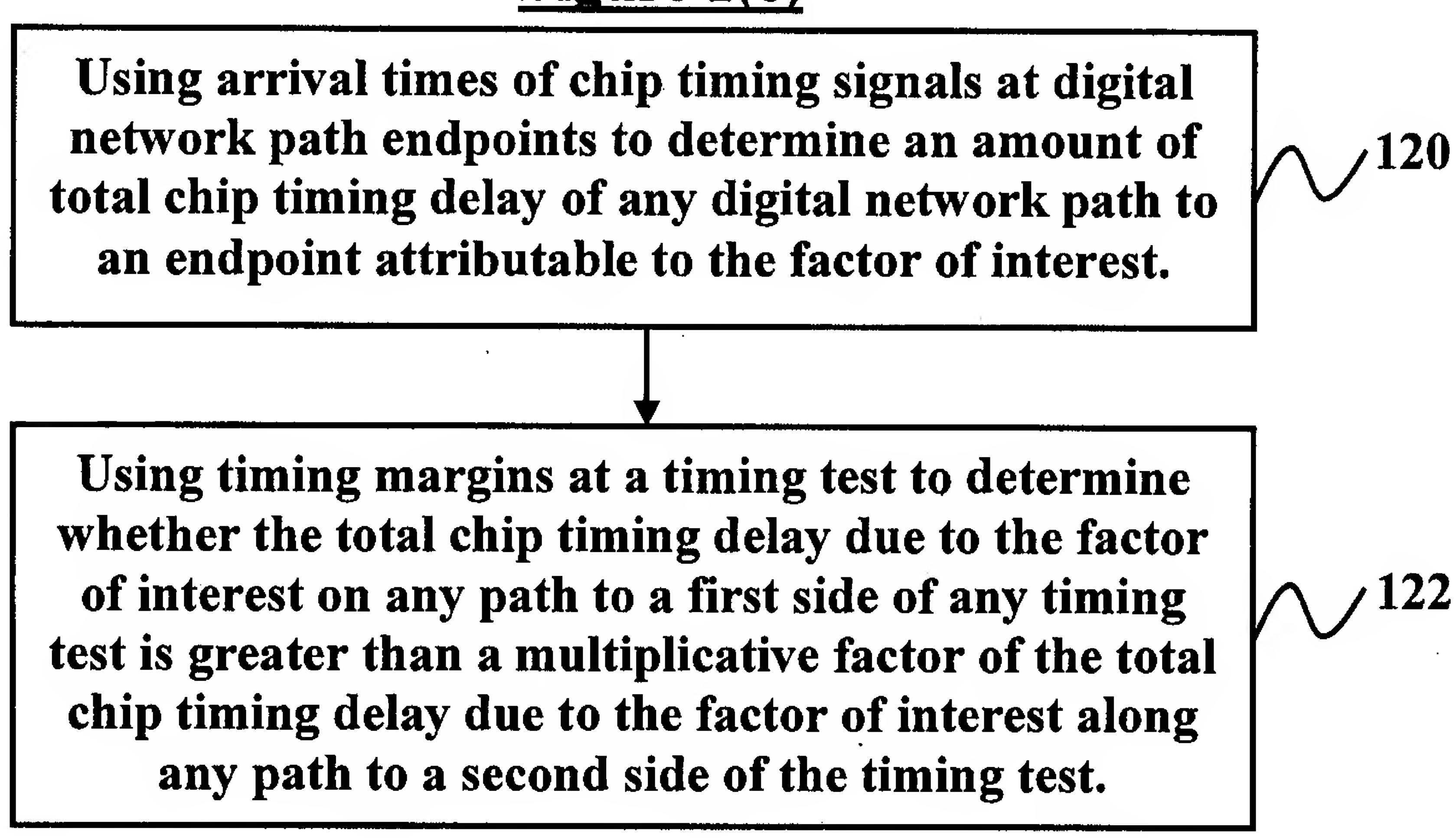


Figure 1(d)

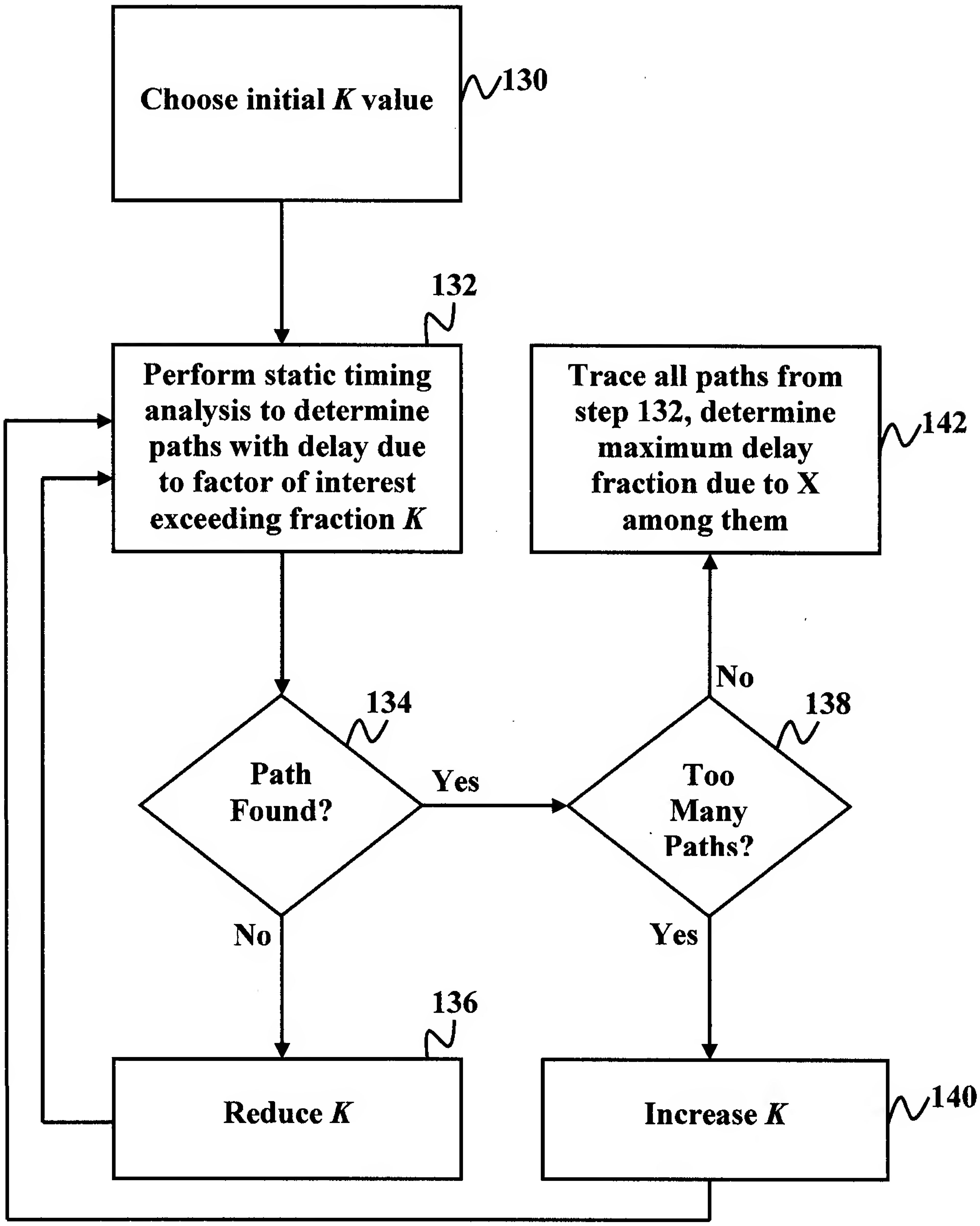

Choose initial *K* value
130
132
Perform static timing analysis to determine paths with delay due to factor of interest exceeding fraction *K*
Trace all paths from step 132, determine maximum delay fraction due to X among them
142
134
Path Found?
Yes
No
138
Too Many Paths?
No
Yes
136
Reduce *K*
Increase *K*
140

Figure 2

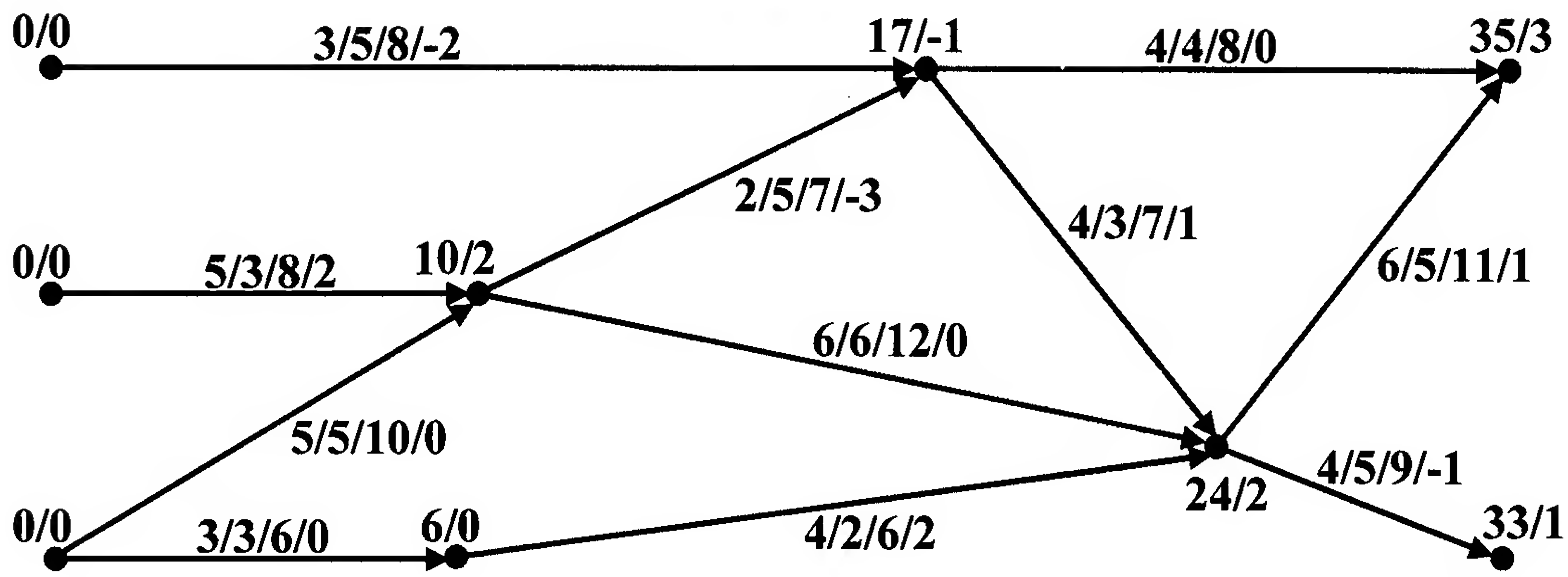


Figure 3

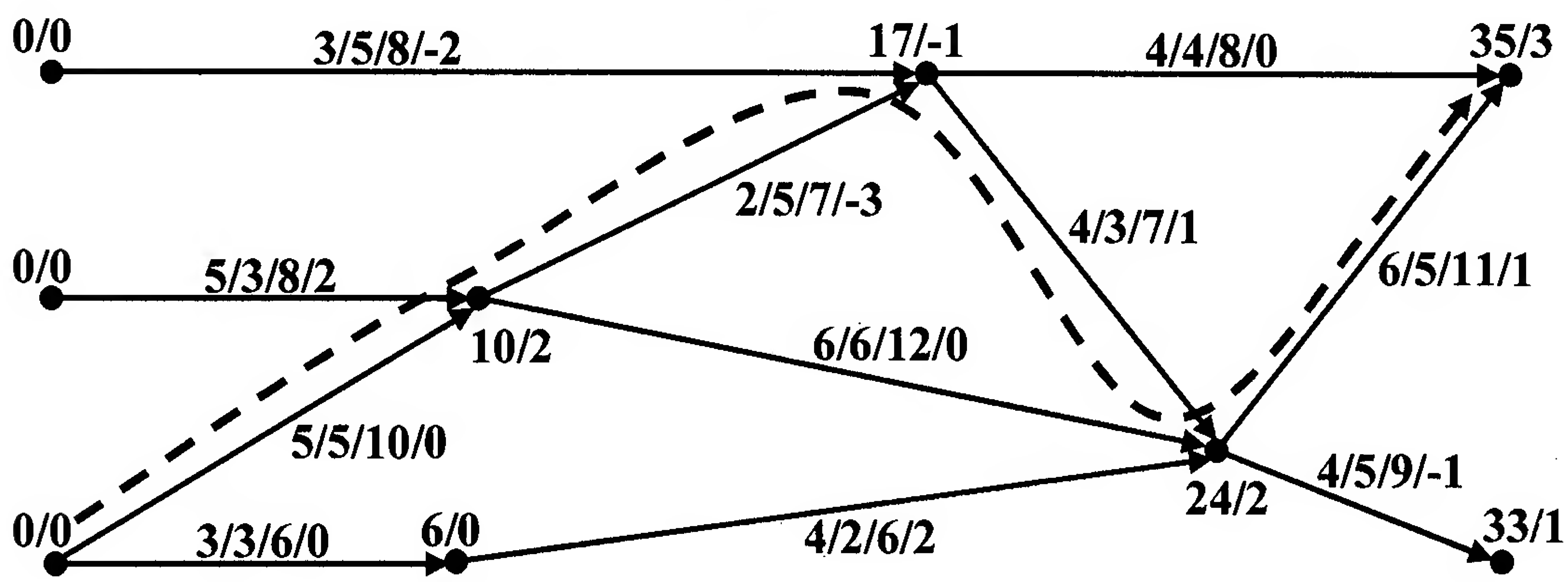


Figure 4

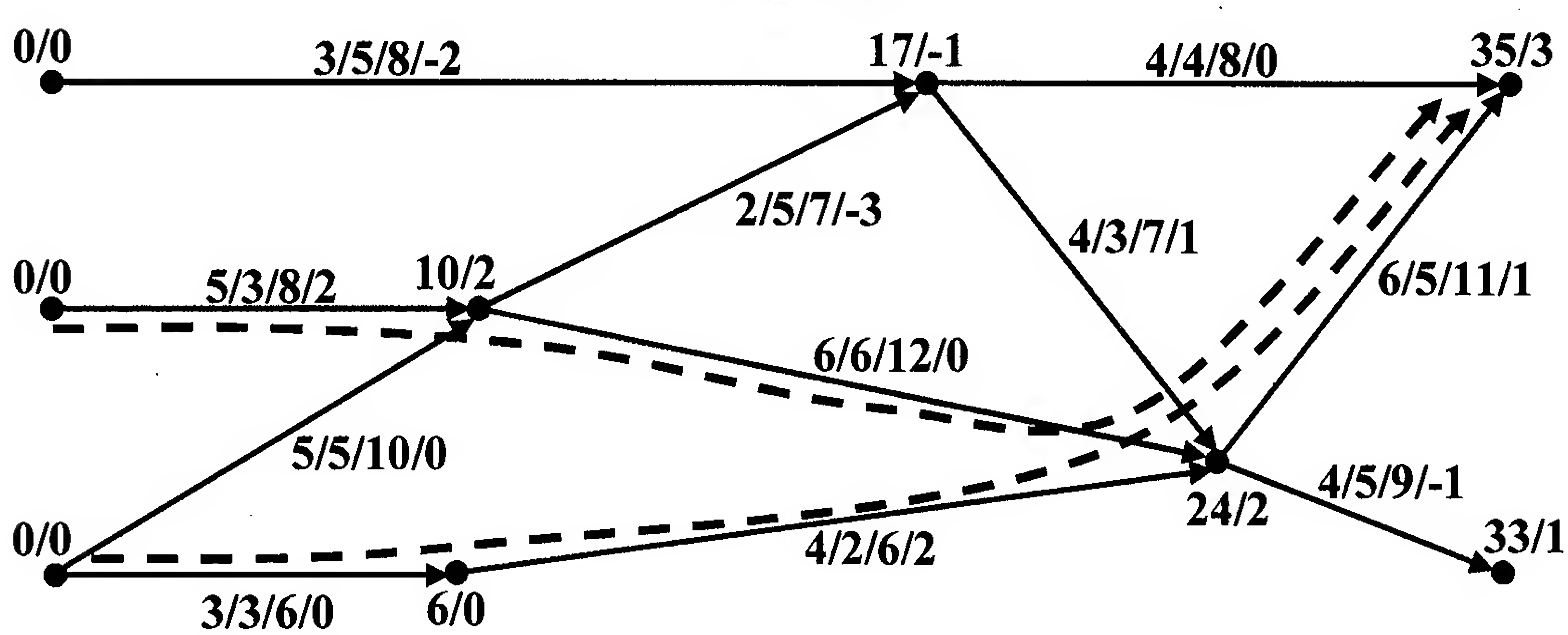
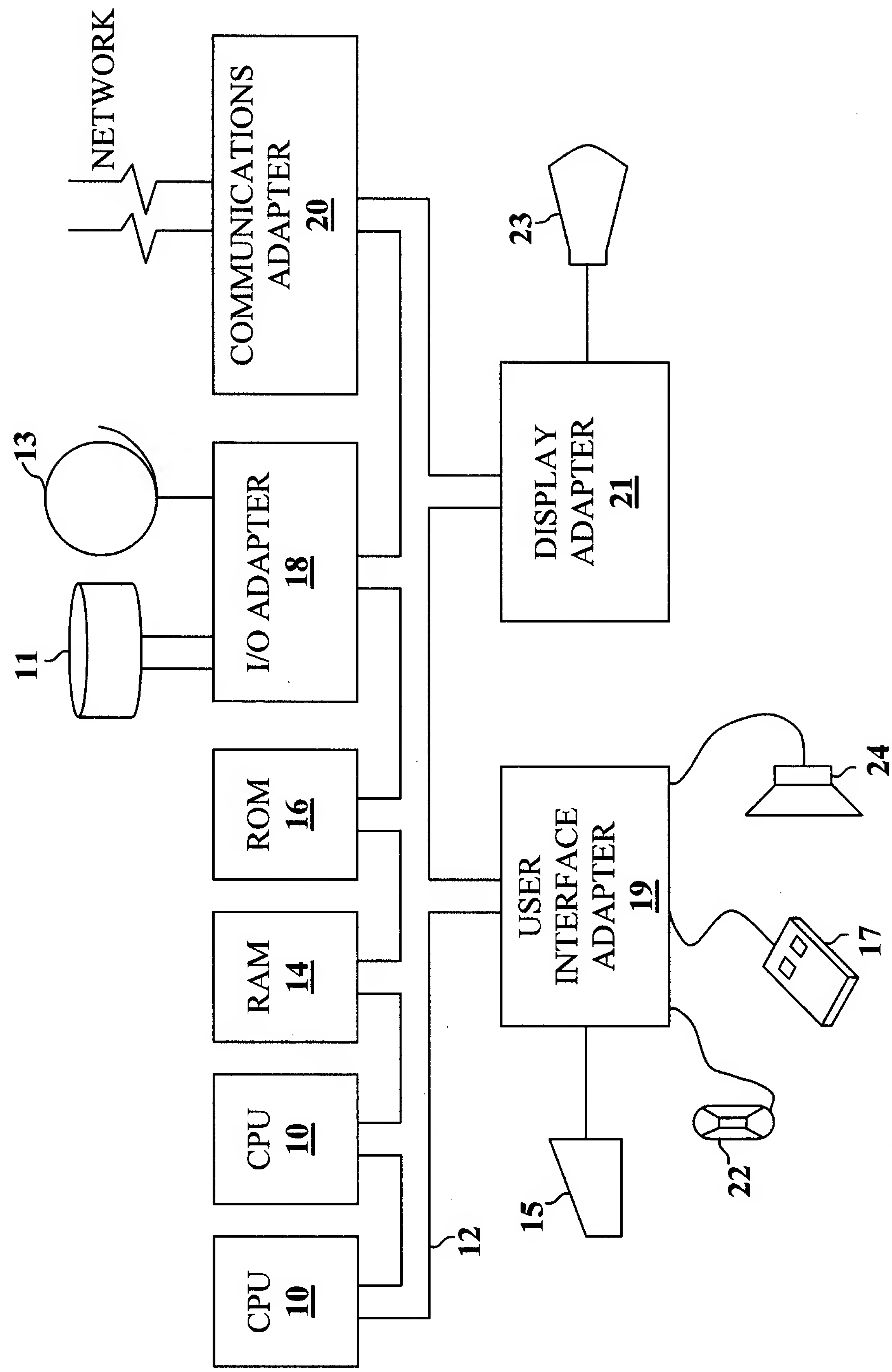


Figure 5


NETWORK
COMMUNICATIONS ADAPTER 20
13
11
I/O ADAPTER 18
ROM 16
RAM 14
CPU 10
CPU 10
12
23
DISPLAY ADAPTER 21
24
USER INTERFACE ADAPTER 19
17
15
22